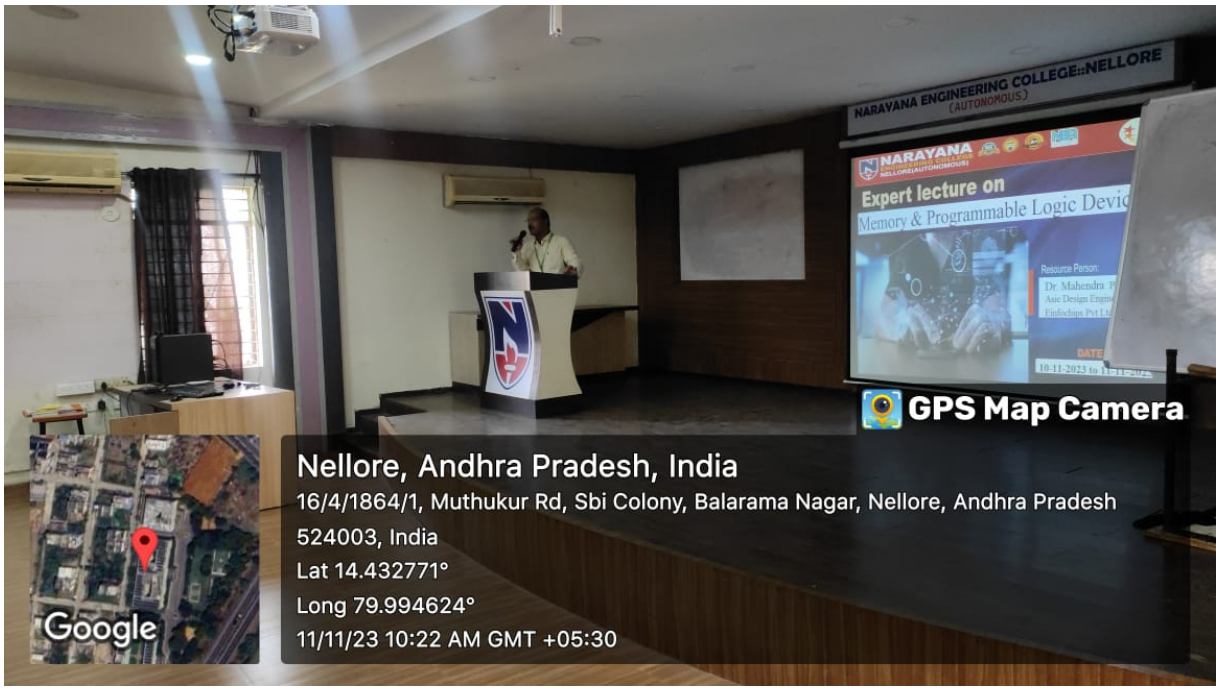
NARAYANA ENGINEERING COLLEGE
NELLORE(AUTONOMOUS)

APPROVED BY AICTE AND PCI NEW DELHI AND AFFILIATED TO JNTUA ANANTAPURAMU
A PART OF NARAYANA GROUPEDUCATIONAL OF INSTITUTIONS, INDIA.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

1	Name of the Activity/Event	Expert Lecture on "**Digital Logic Design**"		
2	Date of Activity/Event	**10/11/2023 to 11/11/2023**		
3	Organized by	**Department of Electronics And Communication Engineering**		
4	Place of Activity/event	Visvesvaraya Auditorium		
5	Resource persons / guest / organization	**Dr.V. MAHENDRA** Sr. Physical Design Engineer, ASIC Division, Bengaluru.		
6	Type of activity/Event	Expert Lecture		
7	Activity/Event objectives	1. This course aims at providing an opportunity for students to enrich their knowledge and skill in developing various solutions for solving engineering problems in the society. 2. This program serves as a platform for students to work with recent trends in Electronic simulation related areas.		
8	Participation	Students	Faculty	Total Participation
		215	-	215
9	General remarks	1. Introduction to Memory & Programmable 2. Study of Logic devices.		
10	Suggested Improvements	Need Hands-on session and more real time examples		
11	Enclosures	1. Program report with Snapshots 2. Attendance sheet		
12	Signature of Co-ordinator			

The **E**lectronics and **C**ommunication **E**ngineering department has organized an Expert Lecture on "**Digital Logic Design**" from **10/11/2023 to 11/11/2023**. The Resource person is **Dr.V. MAHENDRA,** Sr. Physical Design Engineer, ASIC Division, Bengaluru. The students of II B.Tech from the ECE department had attended this Lecture. Total of 215 students attended to this session.

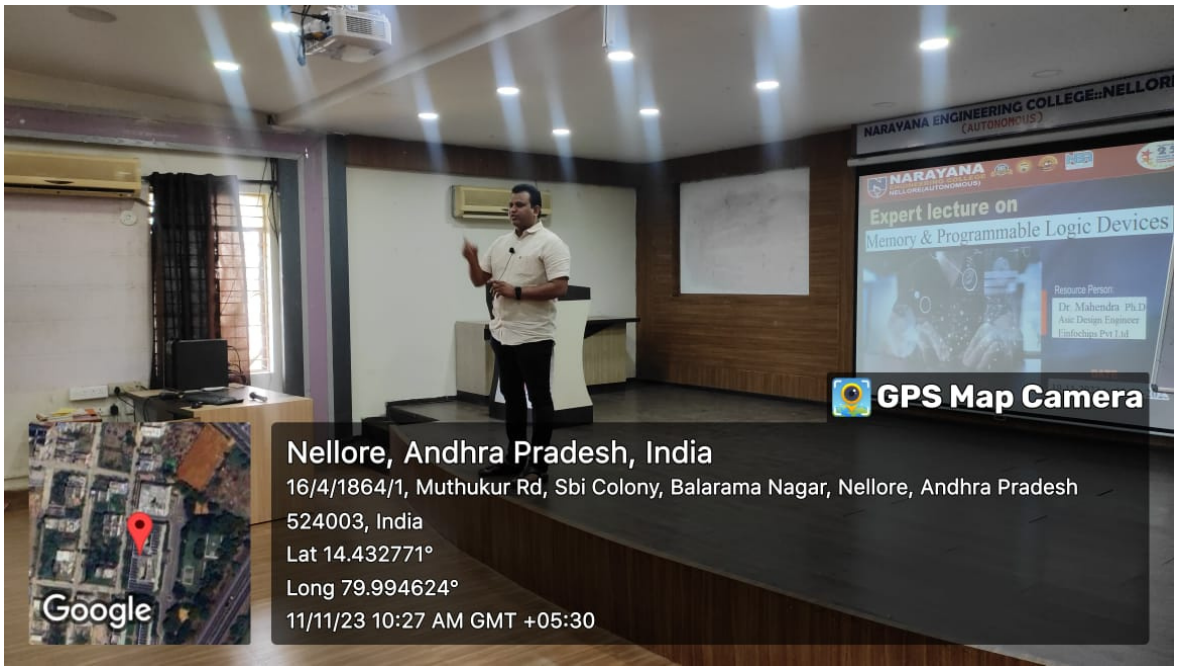


Dr. K. Murali, Head of the Department Introducing Resource person Dr. V. Mahendra

In the first session of lecture resource person, Dr.V. Mahendra briefly discussed about syllabus which was related to their curriculum. On the first day of expert lecture topics covered by resource person are:

- **RAM** (Random Access memory)
- **Types of RAMs** (Static RAM and Dynamic RAM)
- **Memory Decoding**
- **ROM** (Read only Memory)
- **Types of ROMs** (PROM, EPROM, EEPROM)
    - Read-only memory or PROM: blown fuse /fuse intact
    - Erasable PROM or EPROM: placed under a special ultraviolet light for a given period of time will erase the pattern in ROM.
    - Electrically-erasable PROM (EEPROM): erased with an electrical signal instead of ultraviolet light.

- **Flash Memory**



Resource Person giving introduction on topic Memory & Programmable logic devices

On the second day of Expert lecture resource person covered the topics Programmable Logic devices (PLDs) and structure and design of Program logic devices (PLDs) – PROM, PAL, and PLA for different examples.

A combinational PLD is an integrated circuit with programmable gates divided into an:

AND array and an OR array to provide an AND-OR sum of product implementation.

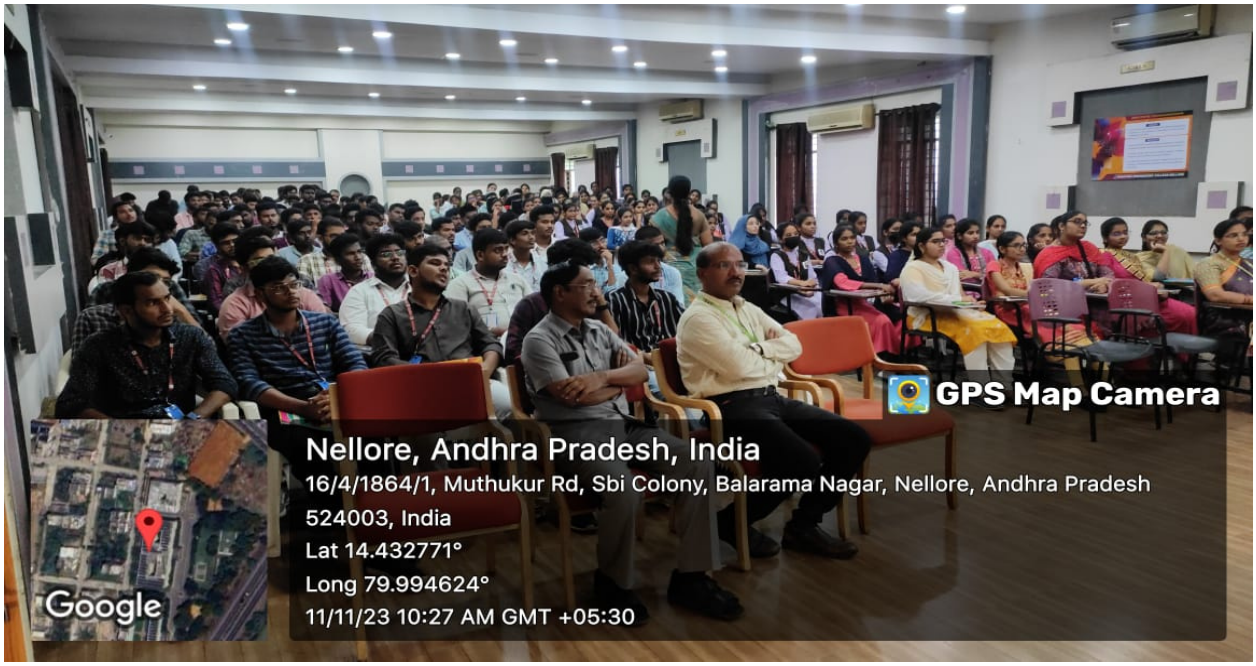
PROM: fixed AND array constructed as a decoder and programmable OR array.

PAL: programmable AND array and fixed OR array.

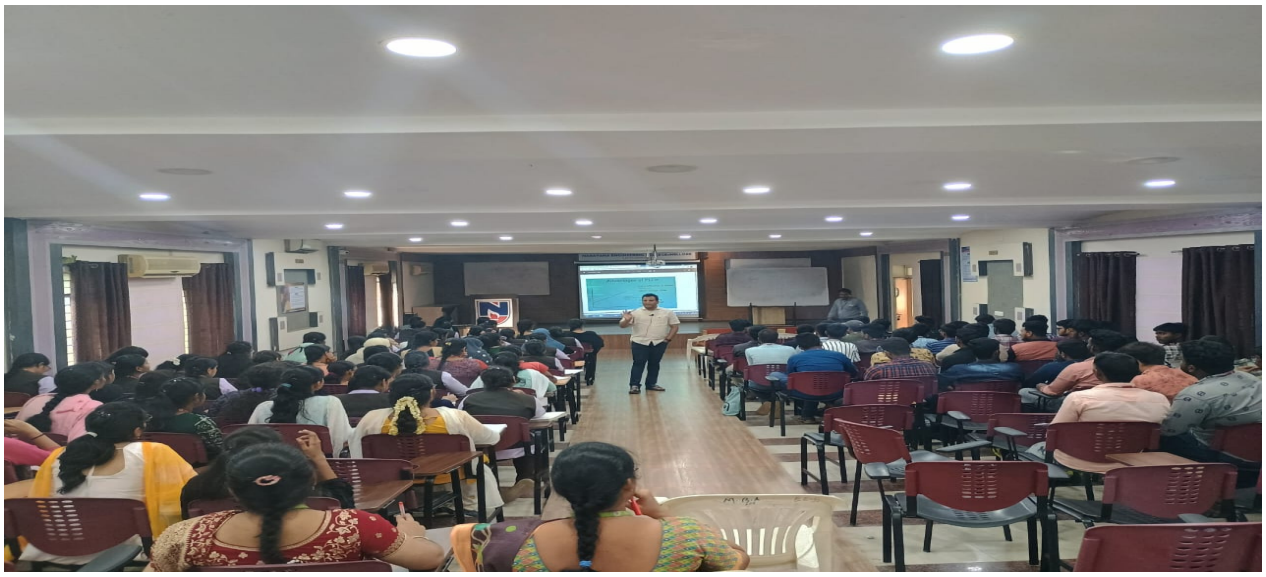
PLA: both the AND and OR arrays can be programmed.

The required paths in a ROM may be programmed in four different ways.

Mask programming: fabrication process



Lecturers and Students Participated in the session



Resource person sharing information regarding the session

Resource person discussed with real time examples and the session was made really interactive by providing an opportunity to suggest a solution to real life scenario with the help of images and videos.

HOD-ECE